High Speed Power Efficient Dynamic Comparator with Low Power Dissipation and Low Offset

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Abstract: When designing digital circuits with high speeds, dynamic comparators are necessary. In particular, central processing units (CPUs) in a wide variety of electronic devices rely on low-power, high-speed dynamic comparators. Numerous comparators, which are comparison circuits, make up these central processing units. This research article introduces a low-voltage, low-power Double Tail Dynamic Comparator (DTDC) that uses less power than previous designs. This journal article compares and contrasts the suggested design with several kinds of dynamic comparators. The suggested architecture is contrasted with dynamic comparators that rely on techniques such as regenerative latch, floating inverter amplifier, and Double Tail. The Tanner EDA simulation program is used to model this design using 18nm technology. This suggested design use the self-biasing approach to execute the pre-amplification process. This suggested design operates with less kick back noise thanks to the self-biasing mechanism.

1. Introduction

These days, faster and more power-efficient comparators are necessities for Analog-Digital converters (ADCs). As a result, the CMOS manufacturing sector is facing increasing demands for the creation of comparators with low power consumption and fast speed. Because of its low static power consumption and high input impedance, the latch type dynamic comparator is especially desirable. [1] The initial step of every contemporary comparator's procedure is a dynamic pre-amplification. What happens in the pre-amplification stage is transferred to the regeneration stage thereafter. Initial development efforts focused on creating dynamic comparators with a single step. A preamplifier circuit and a latch circuit are linked in series in single-stage dynamic comparators. The design, however, had a flaw. The capacitive route between the input and output nodes causes kick-back noise. Because of this kick-back noise, single-stage dynamic comparators were deemed less effective in terms of power consumption compared to subsequent, more efficient models. As stated in [1], energy-efficient gates may be used to create these dynamic comparators. There are now many different kinds of dynamic comparators. A powerful arm latch kind of comparator was one of them. Regenerative comparisons often make use of these strong arm type latch comparators [2]. Because of its robust positive feedback, this strong-arm comparator type has reduced static power. There is only one step to the creation of this sort of comparator. As stated in [3], strong arm latch type comparators provide a lot of voltage headroom due to their one stage architecture. The kick-back noise was controlled by introducing two-stage dynamic comparators. The dynamic two-stage comparator is composed of two distinct phases. The pre-amplifier stage is the first component of a two-stage dynamic comparator[10, 11]. A two-stage dynamic comparator has a latching stage as its second stage. The input signal is initially amplified in the preamplifier circuit. To boost comparison speed while decreasing comparison time, a pre-amplifier amplifies the input signal. Typically, a circuit with back-to-back inverters makes up the second step, the latching circuit [6-8]. at a two-stage dynamic comparator circuit, the comparison is carried performed at the second step.

2. Literature Review

A quick and space-efficient scalable N-bit digital comparator This study presents an N-bit digital comparator that is space-efficient, fast, and uses little power. The proposed comparator architecture consists of two separate components. The first module is the final assessment (FM), and the second is the comparison evaluation (CEM). A parallel prefix tree structure is built using the regular structure of recurring logic cells in the phases of CEM that are independent of the bitwidths of the input operands. The results of the CEM are used by the FM to confirm the previous comparison. Area may be determined by adding up all the transistors and total input-output delay by varying the input operand bit width; this is possible since the proposed structure employs a standard very large-scale integration architecture. The Spectre simulation results at 1 GHz were shown using complementary metal-oxide-semiconductor technology with a CMOS technology. A minimum of 0.57 ns for input-output latency, 9.5 ns for fan-out-of-4 delay, and 1.03 mw for low-power dissipation were features of the proposed comparator, which stood in contrast to earlier designs that relied on 180 nm CMOS technology for 64-bit comparison.
A 1V Low-Power Dynamic Comparator This research presents a power-efficient dynamic comparator for ultra-low power applications. The prototype, built in a 65nm CMOS process with a 1V voltage source, is compared to the frequently used double tail latch comparator in terms of battery life and input referred rms noise. This reduces battery consumption without compromising audio quality. The proposed comparator achieves a referred rms sound level of 220μV, which is 30% lower than the usual comparator, according to the results. However, just 0.19 pJ of electrical power is required by the proposed circuit.
An In-Comparator Aperture-Time Equalisation 7 nm FinFET CMOS 40Gb/s Receiver The in-comparator aperture-time equalisation method is introduced in this study by making use of the impulse response of a timed comparator. This idea is put into practice in a prototype wireline link receiver that uses CMOS 7nm FinFET technology. The recommended method controls the slicers' aperture properties by adjusting the impulse sensitivity functions. This demonstrates an aperture skew adjustment range of 4.7ps to 147fs for NRZ signals at 40Gb/s. Additionally, PAM4 signalling @ 80Gb/s is shown using the proposed approach. These results show that dense I/O networks having fine-grained aperture-time skews in each comparator are feasible for next-generation source-synchronous chip-to-chip systems.
Designs of Fast Comparators for Quick Binary Comparison Here, we present two separate digital comparator architectures that run in parallel. After these comparators are realised in Verilog & modelled on the Xilinx ISE 8.2i platform, they are compared to the traditional design. Results from the simulation show that the first proposed architecture is 23.769 percent faster than the traditional design in terms of mixed delay (logic + connection), and that the subsequent architecture is 35.218 percent faster still.
A Power-Efficient Substitute The Floating-Inverter Amplifier Method This article presents a design for a more energy-efficient comparator. In order to increase gm/ID and decrease noise, the pre-amplifier's inverter-based output pair is powered by a floating reservoir capacitor. This allows for current reuse or dynamic bias. It also makes a big dent in the process corner and input common-mode voltage's influence on the comparator's performance—delays, noise, and offset included. The 180 nm prototype comparison uses just 1 pJ for each comparison while operating on a 1.2 V supply, resulting in 46 μV input-referred noise. This improves energy efficiency by a factor of seven more than that of a strong-arm (SA) lock. As far as we are aware, it has the highest recorded comparative energy efficiency.

3. Existing Method

Figure 1 is a schematic representation of the comparator as described in [5]. We chose this comparator to test our design against because of how fast it is and how well it works with low supply voltage. For the duration of this article, it will be used as a reference comparator. Fig. 2 shows the short-term behaviour of these comparators under the assumption that VP is greater than VN. The OUT+ and OUT- output nodes are discharged to the ground when the clock is low. Assuming certain input voltages VN and VP, the output nodes are charged at various rates by the currents flowing through M3 and M4, respectively, when the clock turns on high. In an NMOS device, a feedback process begins when an output voltage hits a threshold voltage Vth n; in the end, both outputs evaluate to VDD - grounded. The time difference between the 50% levels of the clock and the output, as illustrated in Figure (a), is the delay time. A two-part delay time, t0, and a latch time, t latch, may be expressed as the product of the two variables to and from the equations (1) and (2), respectively, according to the study in [10].

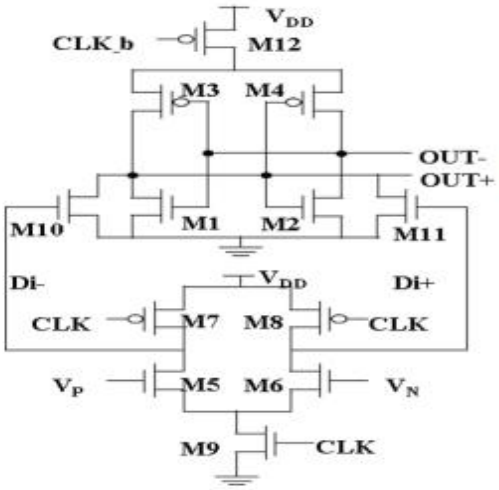


Figure 1. A conventional comparator [5].

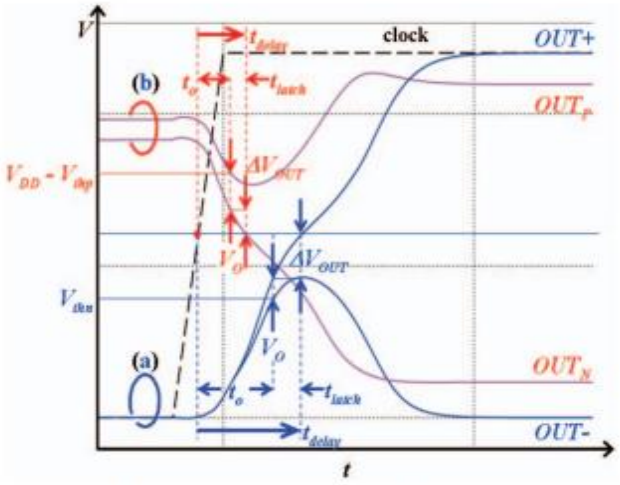


Figure 2. Transient behavior of (a) conventional design [5] (b) proposed design.

$$t_0 = \frac{C_L V_{Charge}}{I_{Eq}} \tag{1}$$

where C_L is the load capacitance at an output node and I_{Eq} is the resultant current of M3 minus the current of M10 and V_{Charge} is equal to V_{thn} in this case.

$$t_{latch} = \frac{C_L}{gm_{eff}} \ln\left(2\frac{\Delta V_{OUT}}{V_O}\right) \tag{2}$$

where ΔV_{OUT} and V_O are as indicated in Fig. 2.

In general V_O can be written as $V_O = G\Delta Vin$ where G is the gain of the interface stage (M5-M11) between the inputs signals and inputs of the cross-coupled inverters and ΔV_{in} is the difference between the input signals (V_P, V_N).

The total delay can be expressed as:

$$t_{delay} = \frac{C_L V_{Charge}}{I_{Eq}} + \frac{C_L}{gm_{eff}} \ln\left(2\frac{\Delta V_{OUT}}{G\Delta Vin}\right) \tag{3}$$

The gain value of the interface between the stage or V Charge may be used as parameters for control to reduce the comparator's latency, as shown in Equation (3). Our primary focus is on high-frequency PRBS chip sampling, where speed is of the utmost importance. The construction of a comparator with high speed makes use of both V Charge & G. Figure 3 shows the two steps that make up the suggested comparator. Transistors M1–M4 and M9 make up the amplification stage, the first step. The regeneration stage, which includes transistors M5–M8 and M10, is the second stage. The amplification and regeneration (or assessment) stages of the circuit are its two main functional units. Transistors M1–M4 form a distinct amplifier with a resistive load by using the on impedance of transistors M3 and M4, as seen in red in Figure 2, during the amplification phase of the clock (CLK). At this point, the regeneration stage's inputs are fed the differential outputs, which are an amplification of the VP/VN difference. Additionally, the regeneration stage cannot be activated since the second tail transistors M10 is turned off. M9 disables the amplification stage's functionality when the clock reaches its high state. In contrast, the regeneration step may now function thanks to the activation of M10. An amplified form of the divergent inputs VN & VP provide the inputs to the regeneration stage, which begins its function. Equation (1) also states that the charging time t0 may be effectively reduced if the amplifier stage is

configured to generate an output close to VDD-|Vthp|. In addition, t latch is often reduced since the gain associated with the gain phase is greater than one. Figure 2(b) shows the suggested circuit's timing diagram, whereas Figure 2(a) shows the reference comparator from [5]. The suggested circuit significantly reduces the delay time compared to the Ref comparator, as seen in this picture. Compared to the reference comparator design, the suggested circuit has a greater energy consumption rate due to the amplification stage's static power usage. But, as will be demonstrated within the following sections, the electrical power usage of the circuit at issue gets equivalent to that of the reference comparator due to its high frequency operation.

4. Proposed Method

Figure 4.1 depicts a typical dynamic comparator that is completely differential. At its highest point, the comparator has an inverter latch and two differential pairs that are cross-coupled. When the Øclk gets high, the inverter currents, which are connected to the inputs, are used to do the comparison. You may alter the trip point by adjusting the size of the input transistors. There aren't many noteworthy issues with this framework that need mentioning. The typical differential comparator's initial flaw has to do with the tail current's clocking. Assuming each differential pair's inputs are known, the tail current enters a linear zone when the clock signal is strong. The two inverter tail currents won't be identical, leading to a significant offset for the comparator, if there are any imperfections or inconsistencies (from a symmetry perspective). A differential pair's inputs are at the heart of the second issue. When there is a big voltage differential between the two inputs to a differential pair, one of the MOSFETs in the pair will flip on and the tail current will be sucked into the other MOSFET. It follows that the comparator will not be comparing differential Vin with differential Vref, but rather Vin + with Vref + (or Vin - with Vref -). The prior code dependant biassed choice may have had a third possible issue. This may occur if one of the comparator's nodes still has a residual charge imbalance from an earlier judgement, which could influence the subsequent choice. In the section that follows, we provide a novel dynamic comparator that overcomes the aforementioned shortcomings of the conventional differential pair comparator.

The source of current transistors NM6 so NM7 are turned off and there is no current channel between the power voltages while the comparator is idle, which is shown by the clk being at OV. The outputs are reset when transistor PM1 and PM4 in the PMOS switch are shorted to Vdd at the same time. The latch's NMOS transistors, also known as NM0 and NM1 are responsible for conducting current and forcing the input transistor NM2 through NM5 to have their drains connected to the Vdd potential. After clk reaches Vdd, the positive supply is severed from the outputs and the switched current sources NM6 & NM7 reach saturation and start conducting. Here we can see the dynamic comparator's waveform. The reference voltage is 500 mV in this case. Logic 0 should be output at voltages below 500 mV. Additionally, logic1 should be output after the reference voltage. Moreover, the input voltage is varied from -1V to 1.8V. As shown in Figure, the Dynamic comparator's waveform.

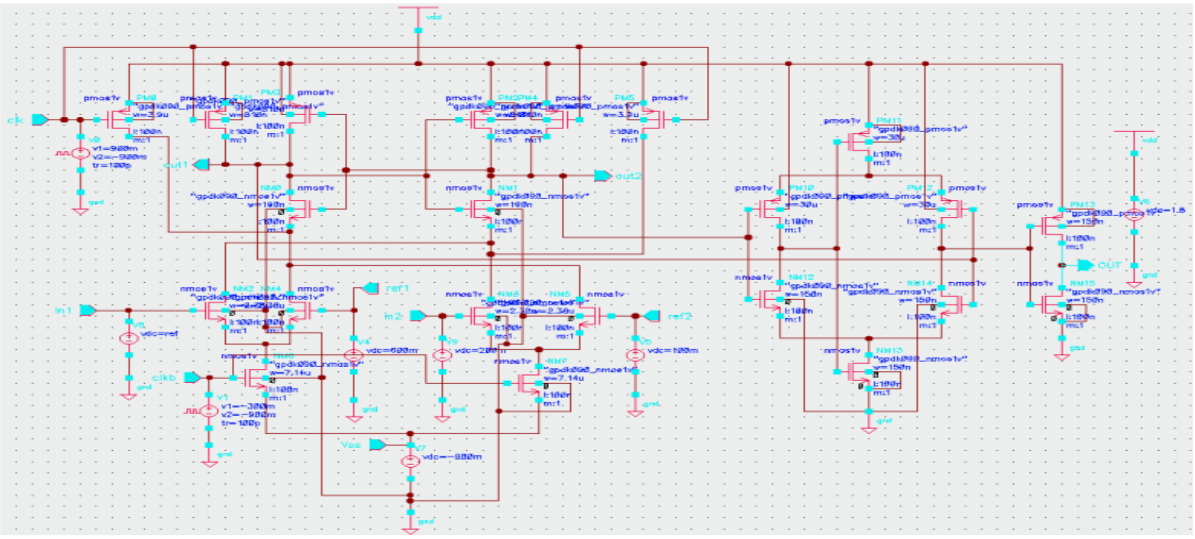


Fig. 3 Dynamic comparator circuit.

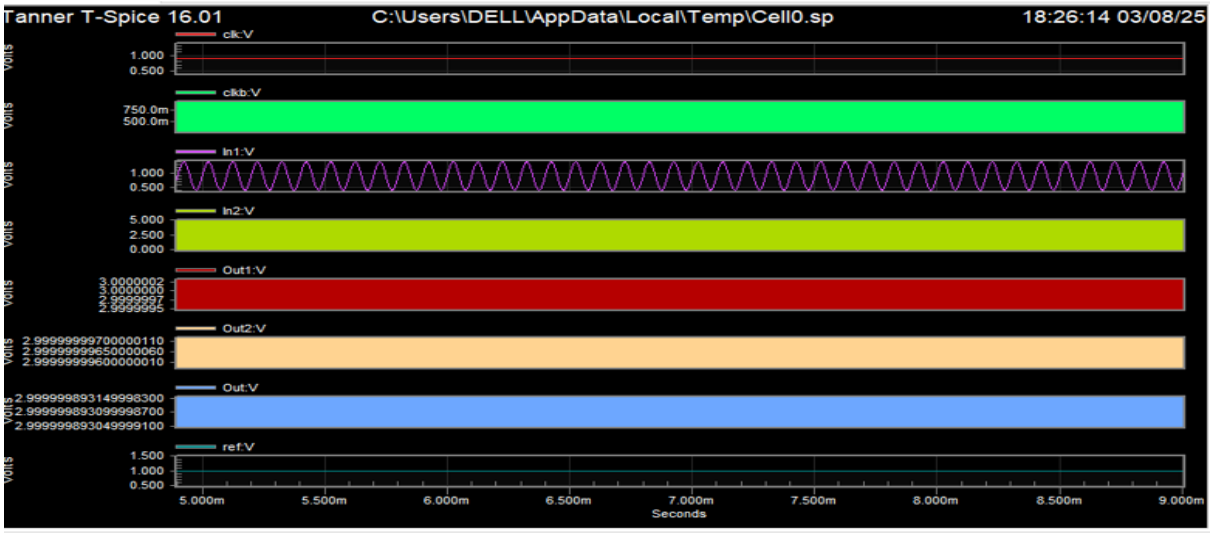
Figure displays the structure of the dynamic comparator. The choice is also taken when the Øclk gets high, just as in the ordinary scenario, when this dynamic comparator is operating. At the moment when the inverter electrical currents are equal, the comparator will be meta-stable. There have been minimal alterations to this structure in comparison to the standard structure. The tail present clock signal is the first component to be modified. A voltage move clock (Øclk,B) that is phase restricted, meaning its high value is less than VDD, has been employed instead of the top switches' clock, which goes from VSS to VDD. This clock can be easily made from the main clock by employing a resistor ladder or an inverter with a desired high voltage. The difference pair tail current is kept in the saturation zone, not the linear region, by means of the limited swing clock. Therefore, a steady 37 degrees of tail current is attained. In the decision-making process of the comparator, this is crucial. The input signals are the subject of the second adjustment.

It has been noted that in a standard differential pair comparator, comparing two signals instead of their differential signals occurs because one of the input transistors [3] is disabled when the input differential is big. One differential pair is coupled with Vin + and Vref + (and Vin - and Vref -) to solve this issue, instead of using Vin + and Vin - (and Vref + and Vref -). Therefore, if there is no imbalance and all the input semiconductors have the same size, the current flowing through transistors NM0 or NM1 will be equal, and the same will be flowing through transistors NM2 and NM3 at the comparator's trip point. So, in order to make a call, the currents from each of the four input transistor will be considered.

Key Conclusions about Dynamic Comparators:

1. High-Speed Performance: For high-frequency applications such as data transmission, analog-to-digital conversion (ADC), and other types of real-time signal processing systems, dynamic comparators are crucial due to their optimised functioning for speed.
2. Low Power Consumption: This kind of comparator is ideal for power-sensitive applications such as cell phones or energy-efficient systems because it uses dynamic circuit approaches instead of static ones, which results in lower power consumption.
3. Improved Noise Immunity: When compared to static comparators, dynamic comparators usually have superior noise rejection. When dealing with tiny signal fluctuations or in settings with high levels of electromagnetic interference (EMI), this becomes even more crucial.
4. Faster Decision Time: Quick transitions among signal states are essential for crucial applications like ADCs, and these comparators' dynamic functioning allows them to resolve input signal discrepancies extremely rapidly, giving shorter decision times.
5. Challenges in Design: Time and dynamic components, including clocking and charge storage, make dynamic comparators more difficult to design. Stability and the minimisation of mistakes like metastability and inappropriate timing need meticulous design.
6. Applications: Many high-speed systems rely on dynamic comparators for quick and accurate signal comparison, such as ADCs, frequency counters, and phase-locked loops (PLLs).

5. Simulation Results



Fig(a)

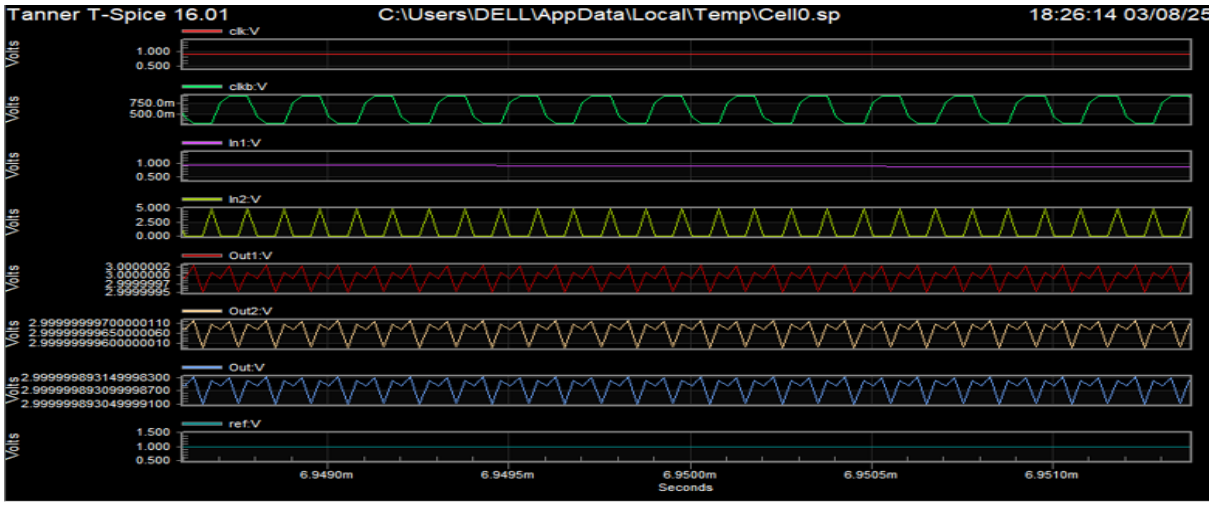


Fig.(b)

Fig(a), Fig(b) are the simulation results of the Dynamic comparator circuit.

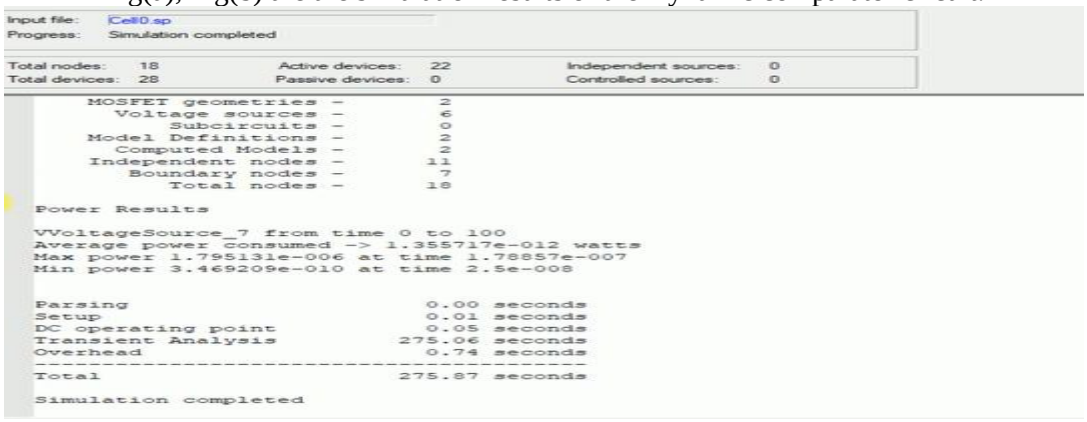


Fig.(c). Transient analysis of the dynamic comprator circuit.

TABLE 1: COMPARISION TABLE

PROCESS	POWER	OFFSET VOLTAGE
Conventional Comparator	461µW	_
Proposed Dyanamic Comparator	1.795µW	3.72mV

6. Conclusion

An example of a high-speed comparator is a dynamic comparator, which compares two input signals using dynamic, or time-dependent, approaches. Dynamic comparators are perfect for high-speed applications due to their reduced power consumption and quicker reaction times compared to standard static comparators. For applications requiring high performance and speed, dynamic comparators are the way to go because to their many benefits in these areas, including reduced power consumption and increased speed. Despite the many advantages, their design need close scrutiny to guarantee dependable performance, especially in settings where noise is a concern or when frequencies are high.

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